

CONFERENCE PROGRAM



**23rd International Symposium
On Power Semiconductor
Devices and ICs**

**Paradise Point Resort
San Diego, California USA
May 23 - 26, 2011**

**Sponsored By:
The Electron Devices Society of The Institute of
Electrical and Electronic Engineers**

**Co – Sponsor:
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**Technical Co-Sponsor:
The Power Electronics Society of the Institute of
Electrical and Electronic Engineers (PELS)**

ISPSD'11	
SCHEDULE AT A GLANCE	
SHORT COURSE : SUNDAY, MAY 22, 2011	
7:30-8:30 AM	Short Course Registration
8:30 AM-5:15 PM	Short Course
5:00-7:00 PM	Conference Registration
MONDAY, MAY 23, 2011	
8:00AM-4:00 PM	Registration
8:30-9:00 AM	Opening Remarks and Announcements
9:00-9:45 AM	Plenary 1: Net Zero Energy Buildings Dr. Satyen Mukherjee Philips Research North America, USA
9:45-10:15 AM	Break
10:15-11:00AM	Plenary 2: High-Speed Railways Tetsuo Uzuka Railway Technical Research Institute, Japan
11:00-11:45 AM	Plenary 3: SiC Power Devices Professor Mikael Östling Royal Institute of Technology, Sweden
11:45AM-1:30 PM	Lunch Break
1:30-3:10 PM	Smart Power Technology I
3:10-3:40 PM	Break
3:40-5:20 PM	Smart Power Technology II
6:00-8:00PM	Welcome Reception
TUESDAY, MAY 24, 2011	
8:00 AM-4:00 PM	Registration
8:30-10:10 AM	IGBT-1
10:10-10:40 AM	Break
10:40AM-12:20 PM	IGBT-2
12:20-2:00 PM	Lunch Break
2:00-3:15 PM	Diodes
3:15-5:45 PM	Poster Session
7:00-10:00 PM	Conference Dinner Party
WEDNESDAY, MAY 25, 2010	
9:00-10:15 AM	GaN Power Devices
10:15-10:40 AM	Break
10:40 AM-12:20 PM	SiC Power Devices
12:20-2:00 PM	Lunch Break
2:00-3:40 PM	High-Voltage MOSFET
3:40-4:10 PM	Break
4:10-5:50PM	Packaging and Module Technologies
THURSDAY, MAY 26, 2011	
8:30-10:10 AM	Device and Process Reliability
10:10-10:40 AM	Break
10:40 A-12:20 PM	Smart Power Circuits
12:20-2:00 PM	Lunch Break
2:00-3:40 PM	Low Voltage Power Devices
3:40-4:10PM	Closing Remarks and Award Ceremony
7:00-10:00 PM	Committee Dinner

Chairman's Message

On behalf of the conference committee, it is my great honor and pleasure to welcome you to the 23th International Symposium on Power Semiconductor Devices and ICs (ISPSD'11). The ISPSD brings together power devices and power ICs community experts to further the research and development of power electronics and its applications. The ISPSD has become the world's leading conference in the field of power devices and power ICs due to the wealth of technical work presented and we are looking forward to a great conference this year.

Following last year's very successful conference in Hiroshima, Japan, our conference once again returns to North America, this time to the beautiful seaside city of San Diego, California, one of the world's top travel destinations.

This year there were 164 submitted abstracts and a total of 95 were accepted. The demographic distribution of the submitted papers reflects the true international character of the ISPSD as 21% of the papers were from North America, 45% from Japan and the Asia Pacific region and 34% from Europe. It is noted that submissions from China, Taiwan and South Korea have significantly increased which is a strong indication of our fast growing international community.

The technical program includes three invited plenary talks, 47 contributed oral presentations, and 48 poster presentations. The three plenary talks are: Dr. Satyen Mukherjee from Philips Research North America, USA will talk about "Opportunities and Challenges with Net Zero Energy Buildings," Dr. Tetsuo Uzuka from Railway Technical Research Institute, Japan will talk about "Trends in High-Speed Railways and the Implications on Power Electronics" and Professor Mikael Östling from Royal Institute of Technology, Sweden will talk about

"SiC Power Devices – Present Status, Applications and Future Perspective".

The conference will also offer an exciting short course program in six segments on Sunday, May 22: "Solid State Lighting Technology and Electronics for Displays, General Lighting and Automotive Applications" by Dr. Radu Surdeanu, "Semiconductor Opportunities in PhotoVoltaic (PV) Systems" by Dr. Henk Jan Bergveld, "Power Devices as Key Components for Photovoltaic (PV) Systems - Challenges and Solutions" Dr. Gerald Deboy, "GaN Power ICs and Design Challenges" Dr. Kevin Chen, "Physics, Challenges, and Solutions of Metal Layout Designs for Large-Area Power Devices" Maxim Ershov, and "On-Die Power Delivery" by Dr. J. Ted DiBene II.

To conclude, I would like to thank the ISPSD'11 Organizing and Technical Program Committee and in particular, Dr. Don Disney (Technical Program Chair), Professor John Shen (Publicity Chair), Dr. Sujit Banerjee (Treasurer), Dr. Gary Dolny (Publications Chair), Dr. Hsueh-Rong Chang (Local Arrangements Chair) and Professor Wai Tung Ng (Short Course Chair). It is also with great pleasure that I extend a warm welcome to all of you attending ISPSD'11 in San Diego.

Mohamed Darwish
General Chairman

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TECHNICAL PROGRAM COMMITTEE

Low Voltage and RF

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**ISPSD 2011 Short Course
High Voltage Devices and IC's**

Short Course Chair: Prof. Wai Tung Ng,
University of Toronto

**Sunday, May 22, 2011
Location: Paradise Point Resort Resort,
San Diego, California, USA**

ISPSD 2011	
SCHEDULE AT A GLANCE	
SHORT COURSE : SUNDAY, MAY 22, 2011	
7:30 - 8:30 AM	Short Course Registration
8:30 – 9:45 AM	Solid State Lighting Technology and Electronics for Automotive, General Lighting and Displays Dr. Radu Surdeanu, NXP
9:45 – 10:00 AM	Coffee Break
10:00 – 11:15 AM	Semiconductor Opportunities in PhotoVoltaic (PV) Systems Dr. Henk Jan Bergveld, NXP
11:15 – 12:30 PM	Power devices as key components for Photovoltaic (PV) systems - Challenges and Solutions Dr. Gerald Deboy, Infineon
12:30 – 1:15 PM	Lunch Break
1:15 – 2:30 PM	GaN Power ICs: Technology and Design Challenges Dr. Kevin Chen, Hong Kong University of Science and Technology
2:30 – 2:45 PM	Coffee Break
2:45 – 4:00 PM	On-die Power Delivery Dr. J. Ted DiBene II, Intel
4:00 – 5:15 PM	Physics, Challenges, and Solutions of Metal Layout Designs for Large Area Power Devices DR. Maxim Ershov, Silicon Frontline Technology
4:00-6:00 PM	Conference Registration

Solid State Lighting and Electronics for Automotive, General Lighting, and Displays

Solid State Lighting (SSL) has become in the past years a fast growing research and development topic, as well as a large emerging market. By offering many benefits, such as: energy reduction, better quality of light, reliability and long life, SSL has entered a wide range of application domains, from general illumination, displays to automotive.

The tutorial will offer details on the key technology issues with LEDs (binning, aging and thermal management) and approaches to tackle them, the current developments in circuitry and system level solutions. Further, a preview of the various application domains with their specific requirements will also be given.

Instructor: Dr. Radu Surdeanu, NXP

Dr. Radu Surdeanu is currently leading the NXP Research activities on Solid State Lighting. He received his Ph.D. degree in Solid State Physics from Vrije Universiteit Amsterdam, The Netherlands. In 2000 he joined Philips Research Laboratories first in Eindhoven, The Netherlands then in 2001 in Leuven, Belgium. He worked on CMOS integration for 90nm, 65nm and 32nm nodes and beyond, with focus on topics as ultra-shallow junctions integration and FinFETs. Since 2006 he joined NXP Semiconductors, where his interest shifted towards Solid State Lighting, in particular working on technology solutions for LED drivers for General Lighting, Displays and Automotive domains. He has published over 40 papers in scientific journals and holds 38 patents. ICs.

Semiconductor Opportunities in Photovoltaic Systems

Although the primary component in any PV system is the PV cell itself, electronic components and circuits are also

needed to ensure proper operation of the PV system. These components are often referred to as Balance-of-System (BoS) components and are based on a range of semiconductor technologies. After presenting the main PV cell technologies and characteristics as well as the construction of PV modules, this tutorial gives an overview of which electronic components are needed in a PV system and what their main characteristics are. These components range from bypass diodes placed in junction boxes at the backside of PV modules to power converters. In state-of-the-art systems, a single inverter (DC/AC) is used to convert the DC output power of the PV system to AC power fed to the grid. The tutorial will illustrate how practical issues such as shading and/or contamination of modules will lead to a reduction in output power in this case. Several solution routes to increase output power under these conditions will be compared, which all revolve around adding local DC/DC or DC/AC converters to the PV modules, implementing distributed power-management schemes. Moreover, customer demands for improved monitoring of the behavior of individual components in the PV system and safety concerns will be illustrated, which lead to additional electronic systems as well. This implies that the amount of electronic circuits and components in PV systems is expected to grow in the future, leading to many opportunities for semiconductors in PV systems.

Instructor: Dr. Henk Jan Bergveld, NXP

Henk Jan Bergveld was born in Enschede, the Netherlands, in 1970. He received the M.Sc. degree (cum laude) and the Ph.D. degree (cum laude) in electrical engineering from the University of Twente, Enschede, in 1994 and 2001, respectively. He joined Philips Research Laboratories, Eindhoven, the Netherlands, in 1994. His research interest was modeling of rechargeable batteries to design better battery management systems. This work resulted in his Ph.D. degree and the book *Battery Management Systems – Design by modeling* (Boston, MA: Kluwer, 2002). He is currently a Principal Scientist and team leader power management in the Central Research and Development department with NXP

Semiconductors in Eindhoven. His main research interests include electronics for PV systems, DC/DC converters, battery management systems for electrical vehicles and class-D amplifiers.

Power devices as key components for Photovoltaic (PV) systems - Challenges and Solutions

Based on Dr. Bergveld's contribution on "Semiconductor opportunities in PV systems" this tutorial will take a detailed look on the role of power semiconductor devices in these circuits. Today's string or multi string inverters use typically a combination of IGBTs, High voltage MOSFETs and fast recovery diodes. The tutorial will lead through a number of topologies and discuss the advantages and disadvantages of different device concepts in the various sockets. The tutorial will also evaluate to which extent system advantages such as higher efficiency, higher switching frequency or higher output power can be achieved with new switches based on Silicon carbide. The emerging segment of distributed power management schemes such as Microinverters and MPP trackers pose specific challenges such as high efficiency at low system power and protection from transients from the grid. The tutorial will illustrate the fundamental topologies and put again focus on the role of power semiconductors therein.

Instructor: Dr. Gerald Deboy, Infineon.

Dr. Gerald Deboy received the M.S. and Ph.D. degree from the Technical University Munich in 1991 and 1996 respectively. He joined Siemens Corporate Research and Development in 1992 and the Semiconductor Division of Siemens in 1995. His research interests were focused on the development of new device concepts for power electronics, especially the revolutionary COOLMOS™ technology. Since 2004 he is heading the Technical marketing department for power semiconductors and ICs within the Infineon Technologies Austria AG. He is a Sr. member of IEEE and has authored or coauthored more

than 50 papers in national and international journals including contributions to three student text books. He holds more than 40 granted international patents and has more applications pending.

GaN Power ICs: Technology and Design Challenges

Wide-bandgap GaN-based semiconductor materials are attracting considerable attention as the preferred material for next-generation power electronics applications, owing to their superior properties including high breakdown electric-field, high carrier density, high electron saturation velocity. GaN power devices can be operated at high voltage and current levels with high switching frequencies, and their inherent high-temperature operating capability could significantly reduce the burden on expensive cooling systems. In a complete power management system, besides the core power components (i.e. switches and rectifiers), intelligent control units are also needed to achieve precise adjustment of the output signal for different loading conditions. At the same time, robust sensing and protection blocks are needed to protect the high-performance power devices against over-temperature, over-current and over-voltage conditions. It is thus desirable to develop power IC technology with which on-chip power conditioning and protection circuits can be implemented to provide optimized performance, increased functionality and enhanced reliability. In this short course, a comprehensive discussion will be given on the development of device technologies for implementing GaN power ICs using the low-cost and highly scalable GaN-on-Si platform. Challenges issues in device technology and their effects on the circuit design will be presented. New device technology development focusing on achieving desirable device performance for power applications will be reviewed.

Instructor: Dr. Kevin Chen, Hong Kong University of Science and Technology

Prof. Chen received the B.S. degree from Peking University in 1988 and the PhD degree from University of Maryland, College Park, USA in 1993. From 1994 to 1995, he was a research engineer in NTT LSI laboratories, Atsugi, Japan, engaging in the research and development of functional quantum effect devices and heterojunction FET's (HFET's). From 1996 to 1998, he was an assistant professor in the Department of Electronic Engineering, City University of Hong Kong. Dr. Chen then joined the Wireless Semiconductor Division of Agilent Technologies, Inc., in 1999 working on RF power amplifiers used in dual-band GSM/DCS wireless handsets. In 2000, Dr. Chen joined Hong Kong University of Science and Technology (HKUST), where he is currently an associate professor in the Department of Electronic and Computer Engineering. At HKUST, he has carried out research in wide bandgap III-nitride devices, silicon-based microwave passive components and 3D through-silicon-via interconnects technology, GaN-based MEMS devices, and multi-band reconfigurable microwave filters. Currently, his group is focused on developing GaN device technologies for power management and high-temperature electronics applications.

On-die Power Delivery

Power delivery for systems from consumer electronics to large servers is becoming very challenging. Advanced power management on these platforms, particularly in the high power devices, has been ongoing for some time but much, much more is needed. Until very recently, the problems with on-die power delivery have resulted in low current and low efficiency indicating that it might be a while before this technology was mature enough to be introduced into products. This tutorial will focus on some of the platform level challenges and will discuss what it takes to do on-die power delivery with magnetics for both CE type devices and for high performance silicon applications.

Instructor: Dr. J. Ted DiBene II, Intel

Dr. J. Ted DiBene II is currently a lead silicon power architect at Intel advancing both silicon and system power management. His recent focus has been in power management for microprocessors and other silicon devices including SoC's. Prior to that, Dr. DiBene was the lead architect and senior technologist for a highly advanced integrated silicon power chip inside of Intel. Along with his background in power he has spent a large portion of this time on system architecture. Prior to working at Intel, Dr. DiBene was the chief technology officer at INCEP Technologies, a startup in San Diego. He has been involved in advanced signal integrity, power system management, and platform research and development since the late 80's and has brought many products thru the development process over his career. Dr. DiBene holds a BSEE from UC Santa Barbara as well as an MSEE and PhD in Applied Physics and Electrical Engineering from UC San Diego. He holds 26 patents and has authored over 50 papers in the area of power, signal integrity, and thermal. He is an affiliate professor at the University of Washington and spends his spare time volunteering his time to education of bio-diesel and other energy conservation efforts at high schools.

Physics, Challenges, and Solutions of Metal Layout Designs for Large Area Power Devices

Layouts of multi-layer metallization of large-area power semiconductor devices have a profound effect on device performance and reliability. Metals, vias, and contacts used to route the currents and voltages for source and drain nets impact the metal debiasing, device on-resistance (R_{dson}), current crowding and current spreading, and uniformity of the current distribution over the area of the device. However, the design, analysis, and optimization of the metal layouts is often driven by the

rule of thumb, or by the experimental trial and error method, which is very time consuming, costly, and error-prone. Things are further complicated by multiple and frequently changing design rules and constraints related to both on-chip (metal interconnects) and off-chip (leadframe, package, and PCB) requirements. The lack or scarcity of literature on the subject (both textbooks and research publications) makes the problem much worse, especially for inexperienced designers and engineers. In this tutorial, we will review the basic principles of metal layout design for power devices, analyze the underlying physical effects, and highlight typical mistakes made by the layout engineers. We will also discuss the "best practices" drawn from the analysis, simulation, and optimization of hundreds of real design examples. Finally, we will show how using a dedicated design tool helps to get an insight into the physics of metal interconnects. The goal of this tutorial is to change the status of metal layout design for power devices from being an art (or black magic) known to a few gurus to science and engineering accessible to many.

Instructor: Dr Maxim Ershov, CTO, Silicon Frontline Technology

Maxim Ershov (Senior member IEEE) received M.Sc. degree from Moscow Institute of Physics and Technology in 1989, and Ph.D. degree from Russian Academy of Sciences in 1992 in solid state electronics. His research interests are in the areas of semiconductor device physics, numerical simulation, and parasitic extraction. M. Ershov published over 100 papers in journals and conferences. He has worked at various academic institutions all over the world (Russia, Japan, and USA) prior to moving to the industry sector. M. Ershov's recent experience includes developing innovative semiconductor devices and processes at PDF Solutions, T-RAM Semiconductor, and Foveon. In Silicon Frontline Technology, he is responsible for the software product and business development of mesh-based and meshless field solvers for parasitic capacitance and resistance extraction and simulation.

TECHNICAL PROGRAM

Monday May 23, 2011

8:30am-9:00am

**Opening Remarks and Announcements
ISPSD'10 Best Paper Award**

9:00am-11:45am Session 1 (P1) Plenary

**Chairs: M. Darwish Maxpower Semiconductor
 P. Moens On Semiconductor**

9:00am-9:45am

**Opportunities and Challenges with Net Zero Energy
Buildings:**

Satyen Mukherjee, Philips Research North America,
United States

Buildings represent about 41% of the total energy consumption in the US. One of the milestones set by the US Department of Energy is the development of net zero energy buildings, defined as buildings that generate as much renewable energy each year as they consume. Net zero energy buildings require a wide ranges of technologies, systems, and solutions. Lighting is a dominant load in buildings followed by heating, cooling, ventilation and various plug loads. This talk will address the roles of different technologies, devices and control strategies being developed for net zero energy buildings. These include high efficiency lighting, daylight integration, DC power bus, solar power integration, closed loop integrated control, smart grid interface, and emerging approaches such as chilled beams and active facades. All of these involve power conversion and controls in one form or the other where high voltage or high power integrated solutions are key to commercial viability. In addition to this, the role of whole building modeling and simulation in the development and deployment of the solutions will be addressed.

9:30am-10:15am Break

10:15-11:00 AM

Trends in High-speed Railways and the Implications on Power Electronics

Tetsuo Uzuka, Railway Technical Research Institute,
Japan

High-speed railways are expanding rapidly around the world. These high-speed trains are fed by high-voltage and are equipped with several large motors. In addition, high-speed trains have a strict restrictions for both weight and volume. Thus, high-speed trains need small, light-weight power semiconductors that can handle very high voltages and high currents. High switching speeds and electromagnetic compatibility concerns place additional constraints on these devices. From simple silicon diodes in 1960s, thyristors, GTO thyristors, IGBTs, and emerging technologies such as SiC, the progress of power semiconductor technologies have directly benefitted the performance of high-speed railways. This talk will provide a review of the global expansion and improvement of high-speed railways, with emphasis on the role that power electronics have played in that evolution.

11:00am-11:45am

SiC Power Devices - Present Status, Applications & Future Perspective

Mikael Östling, Royal Institute of Technology, Sweden

This presentation will give a review of the present status of silicon carbide power device technology and discuss the most promising application areas for this technology. A discussion of the various device concepts will be presented, including the major technologies for MOSFETs, JFETs BJT, PN and Schottky diodes. A comparison with present silicon-based power device families such as IGBTs and superjunction MOSFETs will be included. Commercial and research device results will be covered. Some examples of demonstrated and promising gallium nitride power devices will be discussed.

11:00am-1:30pm

Lunch Break

1:30pm-3:00pm Session 2
Smart Power Technology 1

Chairs: Sameer Pendharkar, TI
Tanya Trajkovic, Cambridge Semiconductor

1:30pm-1:55am

A Novel Substrate-Assisted RESURF Technology for Small Curvature Radius Junction:

Ming Qiao, Xi Hu, Hengjuan Wen, Meng Wang, Bo Luo, Xiaorong Luo, Zhuo Wang, Bo Zhang, Zhaoji Li, University of Electronic Science and Technology of China, China

1:55pm-2:20pm

Automotive 130 nm Smart-Power-Technology Including Embedded Flash Functionality:

Ralf Rudolf, Marc Strasser, Matthias Stecher, Infineon AG, Germany

2:20pm-2:45pm

Implementation of Fully Isolated Low Vgs nLDMOS with Low Specific on-Resistance:

Chouljoo Ko, Cheol-Ho Cho, Hee-Bae Lee, Yong-Jun Lee, Min-Woo Kim, Sun-Kyung Bang, Han-Geon Kim, Sun-Kyoung Kang, Nam-Joo Kim, Dongbu Hitek, Korea, South

2:45-3:10pm

Wide-Voltage SOI-BiCDMOS Technology for High-Temperature Automotive Applications:

Hidemoto Tomita, Hiroomi Eguchi, Shinya Kijima, Norihiro Honda, Tetsuya Yamada, Hideo Yamawaki, Hirofumi Aoki, Kimimori Hamada, Toyota Motor Corporation, Japan

3:10 pm-3:40pm Break

**3:40pm-5:20pm Session 3
Smart Power Technology II**

Chairs: T. Letavic, IBM
A. Shibib, Bourns

3:40pm-4:05pm

**New Low Resistance and Compact MOSFET for
Analog Switch ICs with V-Groove Dielectric Isolation:**
Kenji Hara^{1}, Junichi Sakano^{1}, Hironobu Honda^{2},
Junichi Aizawa^{2}, Taiga Arai^{2}, ^{1}Hitachi Research
Laboratory, Hitachi, Ltd., Japan; ^{2}Power Device
Division, Power Systems, Hitachi, Ltd., Japan

4:05pm-4:30pm

**A Novel 0.16 μ m - 300V SOIBCD for Ultrasound
Medical Applications:**
Marco Sambì^{1}, Daniele Merlini^{1}, Filippo
Belletti^{1}, Emiliano Bonera^{2}, Paola
Galbiati^{1} ^{1}STMicroelectronics TR&D, Italy;
^{2}University of Milano Bicocca, Italy

4:30pm-4:55pm

300V Field-MOS Fets for HV-Switching IC:
Tomoyuki Miyoshi, Tatsuya Tominari, Yoshihiro
Hayashi, Atsushi Ito, Takayuki Oshima, Shinichiro Wada,
Hitachi, Ltd., Japan

4:55pm-5:20pm

**High Performance Pch-LDMOS Transistors in Wide
Range Voltage from 35V to 200V SOI LDMOS
Platform Technology:**
Satoshi Shimamoto, Yohei Yanagida, Shinji Shirakawa,
Kenji Miyakoshi, Toshinori Imai, Takayuki Oshima,
Junichi Sakano, Shinichiro Wada, Hitachi, Ltd., Japan

6:00pm-8:00pm Welcome Reception

Tuesday May 24, 2011

**8:30am-10:10am Session 4
IGBT I**

**Chairs: Reinhard Herzer, Semikron
 Yasukazu Seki, Fuji Electric**

8:30am-8:55am

1.7kV Trench HiGT with Deep and Separate Floating-P Layer Designed for Low Loss, Low EMI Noise, and High Reliability:

So Watanabe^{1}, Taiga Arai^{2}, Kohsuke Ishibashi^{2}, Yasushi Toyoda^{2}, Tetsuo Oda^{2}, Takashi Harada^{2}, Katsuaki Saito^{2}, Mutsuhiro Mori^{1}, ^{1}Hitachi Research Laboratory, Hitachi, Ltd., Japan; ^{2}Power & Industrial Systems Division, Hitachi, Ltd., Japan

8:55am-9:20am

Development of the Next Generation 1700V Trench-Gate Fs-IGBT:

Yuichi Onozawa, Daisuke Ozaki, Hayato Nakano, Tomoyuki Yamazaki, Naoto Fujishima, Fuji Electric Systems Co.,Ltd, Japan

9:20am-9:45am

The Radial Layout Design Concept for the Bimode Insulated Gate Transistor:

Liutauras Storasta^{2}, Munaf Rahimo^{2}, Marco Bellini^{1}, Arnost Kopta^{2}, Umamaheswara Vemulapati^{3}, Nando Kaminski^{3}, ^{1}ABB Switzerland Ltd, Corporate Research, Switzerland; ^{2}ABB Switzerland Ltd, Semiconductors, Switzerland; ^{3}University of Bremen, Institute for Electrical Drives, Power Electronics and Devices (IALB), Germany

9:45am-10:10am

Full Digital Short Circuit Protection for Advanced IGBTs: Takuya Tanimura, Kazufumi Yuasa, Ichiro Omura, Kyushu Institute of Technology, Japan

10:10am-10:40am Break

10:40am-12:20pm Session 5

IGBT II

Chairs: Ichiro Omura, Kyutech University
Jean-Louis Sanchez, LAAS

10:40am-11:05am

Ultrathin 400v Fs IGBT for HEVv Applications:

Heike Böving, Thomas Laska, Anton Pugatschow,
Waldemar Jakobi, Infineon Technologies, Germany

11:05am-11:30am

**600V LPT-CSTBTM on Advanced Thin Wafer
Technology:**

Yuki Haraguchi, Shigeto Honda, Kazunari Nakata,
Atsushi Narazaki, Yoshiaki Terasaki, Mitsubishi Electric
Corporation, Japan

11:30am-11:55am

**High Speed 650V IGBTs for DC-DC Conversion Up to
200 Khz:**

Hsueh-Rong Chang, Jiankang Bu, George Kong, Rachana
Bou, International Rectifier, United States

11:55am-12:20pm

**Novel High Voltage LDMOS on Partial SOI with
Double-Sided Charge Trenches:**

Xiao Luo^{2}, Yuan Wang^{2}, Lei Lei^{2}, Tian Lei^{1},
Da Fu^{2}, Guo Yao^{2}, Ming Qiao^{2}, Bo Zhang^{2},
Zhao Li^{2}, ^{1}Monolithic Power Systems, China;
^{2}University of Electronic Science and Technology of
China, China

12:20pm-2:00pm

Lunch Break

2:00pm-3:15pm Session 6

Diodes

Chairs: **Dan Kinzer**, Fairchild
Stefan Linder, ABB

2:00pm-2:25pm

Innovative Designs Enable 300-V TMBS with Ultra-Low on-State Voltage and Fast Switching Speed:

Wesley Chih-Wei Hsu^{2}, Florin Udrea^{1}, Pai-Li Lin^{2}, Yih-Yin Lin^{2}, Max Chen^{2},^{1} Cambridge University, United Kingdom; ^{2}VGST, Taiwan

2:25pm-2:50pm

Ultra Low Loss Trench Gate PCI-Pin Diode with $V_F < 350\text{mV}$:

Motohiro Tsuda, Yasuaki Matsumoto, Ichiro Omura, Kyushu Institute of Technology, Japan

2:50pm-3:15pm

Field Shielded Anode (FSA) Concept Enabling Higher Temperature Operation of Fast Recovery Diodes:

Sven Matthias, Jan Vobecky, Chiara Corvasce, Arnost Kopta, Marta Cammarata, ABB Switzerland, Switzerland

3:15pm-5:45pm

Poster Session

Chairs: **Sujit Bannerjee**, Power Integrations
Ted Latavic, IBM

HV-P1 Evaluation of 1.2kV Super Junction Trench-Gate Cluster Insulated Gate Bipolar Transistor (SJ-TCIGBT):

Luther-King Ngwendson, Sankara Narayanan, University of Sheffield, United Kingdom

HV-P2 Relaxation of Current Filament Due to RFC Technology and Ballast Resistor for Robust FWD Operation:

Akito Nishii, Katsumi Nakamura, Fumihito Masuoka, Tomohide Terashima, Mitsubishi Electric Corporation, Japan

HV-P3 Limits of Strongly Punch-Through Designed IGBTs:

Thomas Raker, Hans-Peter Felsl, Franz-Josef Niedernostheide, Frank Pfirsch, Hans-Joachim Schulze, Infineon Technologies AG, Germany

HV-P4 Filament-Induced thermomigration of an Aluminum Drop at the Cathode Side of High-Voltage Power Diodes:

Hans-Joachim Schulze^{2}, Jürgen Biermann^{2}, Josef-Georg Bauer^{2}, Franz-Josef Niedernostheide^{2}, Josef Lutz^{1}, Roman Baburske^{1},^{1} Chemnitz University of Technology, Germany; ^{2} Infineon Technologies AG, Germany

HV-P5 Optimization of Diodes Using the Speed Concept and CIBH:

Manfred Pfaffenlehner^{2}, Hans-Peter Felsl^{2}, Franz-Josef Niedernostheide^{2}, Frank Pfirsch^{2}, Hans-Joachim Schulze^{2}, Roman Baburske^{1}, Josef Lutz^{1},^{1} Chemnitz University of Technology, Germany; ^{2} Infineon Technologies AG, Germany

HV-P6 Edge Termination Impact on Clamped Inductive Turn-Off Failure in High-Voltage IGBTs Under overcurrent Conditions:

Xavier Perpinya, Ignasi Cortes, Jesus Urresti-Ibanez, Xavier Jorda, Jose Rebollo, Jose Millan, IMB-CNM, Spain

HV-P7 Hybrid Isolation Process with Deep Diffusion and V-Groove for Reverse Blocking IGBTs:

Haruo Nakazawa^{1}, Masaaki Ogino^{1}, Hiroki Wakimoto^{1}, Tsunehiro Nakajima^{1}, David Hongfei Lu^{2}, Yoshikazu Takahashi^{1},^{1} Fuji Electric Holdings Co.,Ltd., Japan; ^{2} Fuji Electric Systems Co., Ltd., Japan

HV-P8 Reduction of the Temperature Dependence of Leakage Current of IGBTs by Field-Stop Design:

Stephan Voss, Holger Huesken, Franz-Josef Niedernostheide, Hans-Joachim Schulze, Infineon Technologies AG, Germany

HV-P9 Electro-Thermal Instability in Multicellular Trench-IGBTs in Avalanche Condition: Experiments and Simulations:

Michele Riccio^{2}, Andrea Irace^{2}, Giovanni Breglio^{2}, Paolo Spirito^{2}, Yoshishito Mizuno^{1},^{1} Toyota Motor Corporation, Japan; ^{2} University of Naples Fededico II, Italy

HV-P10 On Chip ESD Protection of 600V Voltage Node:

Vladislav Vashchenko, National Semiconductor, United States

HV-P11 CSTBTM(III) Having Wide SOA Under High Temperature Condition:

Kenji Suzuki, Tetsuo Takahashi, Tomohide Terashima, Mitsubishi Electric Corporation, Japan

HV-P12 Physical Analysis of Carrier Lifetime

Controlled IGBT:

Chihiro Tadokoro^{2}, Mitsuru Kaneda^{3}, Kazutoyo Takano^{1}, Shigeru Kusunoki^{3}, Tadaharu Minato^{3},^{1}Power Chip Design,Sec.,Design & Technology Dept., Japan; ^{2}Power Chip Design,Sec.,Design & Technology Dept.,Fukuryo Semicon Engineering Corporation, Japan; ^{3}Power Device Works, Mitsubishi Electric Corporation, Japan

HV-P13 High Temperature Wafer Bonding Technique for the Realization of a Voltage and Current

Bidirectional IGBT:

Abdelhakim Bourennane, Jean Louis Sanchez, LAAS-CNRS, France

HV-P14 Effects of Back-Side He Irradiation on MOS-GTO Performances:

Cesare Ronsisvalle^{2}, Vincenzo Enea^{2}, Carmine Abbate^{3}, Giovanni Busatto^{3}, Francesco Iannuzzo^{3}, Annunziata Sanseverino^{3}, Pablo Cirrone^{1},^{1}LNS - INFN Catania, Italy; ^{2}STMicroelectronics, Italy; ^{3}University of Cassino, Italy

HV-P15 Temperature Dependence of Switching Performance in IGBT Circuits and its Compact Modeling:

Masataka Miyake^{1}, Masaya Ueno^{1}, Junichi Nakashima^{1}, Hiroki Masuoka^{1}, Uwe Feldmann^{1}, Hans Juergen Mattausch^{1}, Mitiko Miura-Mattausch^{1}, Takaoki Ogawa^{2}, Takashi Ueta^{2},^{1}Hiroshima University, Japan; ^{2}Toyota Motor Corporation, Japan

LV-P1 Full Understanding of Hot-Carrier-Induced Degradation in STI-Based LDMOS Transistors in the Impact-Ionization Operating Regime:

Stefano Poli^{3}, Susanna Reggiani^{2}, Marie Denison^{1}, Giorgio Baccarani^{3}, Elena Gnani^{3}, Antonio Gnudi^{3}, Sameer Pendharkar^{1}, Rick Wise^{{1}, {1}} Texas Instruments, United States; ^{2}University of Bologna, Italy; ^{3}University of Bologna, Italy

LV-P2 Avalanche Instability in Oxide Charge

Balanced Power MOSFETS:

Joseph Yedinak, Rick Stokes, Dean Probst, Ashok Challa, Suku Kim, Steven Sapp, Fairchild Semiconductor Corp., United States

LV-P3 Prognostics of Power MOSFET:

Jose Celaya^{3}, Vladislav Vashchenko^{4}, Abhinav Saxena^{3}, Sankalita Saha^{2}, Kai Goebel^{{1}, {1}} NASA Ames Research Center, United States; ^{2} NASA Ames Research Center (MCT Inc.), United States; ^{3} NASA Ames Research Center (SGT Inc.), United States; ^{4} National Semiconductor Corp., United States

LV-P4 Modeling the 3D Self Ballasting Behavior and Filamentation Under High Current Stressing in DeNMOS:

Amitabh Chatterjee, Texas Instruments, United States

IP-P1 Low-on-Resistance Strain-Controlled LDMOS Transistors for 0.25-um Power ICs:

Masafumi Miyamoto, Nobuyuki Sugii, Yukihiro Kumagai, Yoshinobu Kimura, Hitachi, Ltd., Japan

IP-P2 0.25µm, 20V High Performance

Complementary Bipolar Transistor with Dual EPI and Oxide-Filled Deep Trench Isolation for High Frequency DC-DC Converters:

Taehun Kwon, Sheldon Haynie, Alexei Sadovnikov, Paul Allard, John Strout, Andy Strachan, National Semiconductor, United States

IP-P3 Integration of 100V LDMOS Devices in 0.35 μ m CMOS Technology:

Paul Stribley, Suba Subramaniam, X-FAB Semiconductor Foundries, United Kingdom

IP-P4 High-Voltage Thick Layer SOI Technology for PDP Scan Driver IC:

Ming Qiao^{2}, Lingli Jiang^{2}, Meng Wang^{2}, Yong Huang^{2}, Hong Liao^{1}, Tao Liang^{2}, Zhen Sun^{1}, Bo Zhang^{2}, Zhaoji Li^{2},^{1} Changhong Electric Co., Ltd., China; ^{2}University of Electronic Science and Technology of China, China

IP-P5 Considerations on the Optimal Power Stage Segmentation Algorithms for MHz Integrated Synchronous Buck DC-DC Converters;

Xiaopeng Wang, Alex. Q. Huang, North Carolina State University, United States

IP-P6 The ESD Failure Mechanism of Ultra-HV 700V LDMOS:

Jian-Hsing Lee, Chien-Ling Chan, Hung-Der Su, Kuo-Cheng Chang, R&D, Taiwan

IP-P7 Thermal Modeling of Box/DTI Enclosed Power Devices with Green's Function:

Kai Moebus^{1}, Yves Zimmermann^{1}, Gerald Wedel^{1}, Michael Schröter^{2},^{1} TU Dresden, Germany; ^{2} TU Dresden, UCSD, Germany

IP-P8 Techniques to Prevent Substrate Injection Induced Failure During ESD Events in Automotive Applications:

Amaury Gendron, Chai Gill, Craig Aykroyd, Carol Zhan, Freescale Semiconductor, United States

IP-P9 IGBT Driver Chip Set with Advanced Digital Signal Processing:

Jan Lehmann, Günter Katzenberger, Gunter Königsmann, Matthias Roßberg, Reinhard Herzer, Semikron Elektronik GmbH & Co. KG, Germany

IP-P10 Solutions to Improve Flatness of Id_Vd Curves of Rugged Nldmos:

Samir Mouhoubi, Filip Bauwens, Jaume Roig, Pierre Gassot, Peter Moens, Marnix Tack, OnSemiconductor, Belgium

IP-P11 The Vertical Voltage Termination Technique – Integration, Insulation and Termination of Single Die Multiple Power Devices:

Kremena Vladimirova, Jean-Christophe Crebier, Yvan Avenas, Christian Schaeffer, G2Elab, France

IP-P12 Investigation of Parasitic BJT Turn-on Enhanced Two-Stage Drain Saturation Current in High-Voltage NMOS Transistor:

Chih-Chang Cheng, H.L. Chou, F.Y. Chu, R.S. Liou, Y.C. Lin, K.M. Wu, Y.C. Jong, C.L. Tsai, H.C. Tuan, Taiwan Semiconductor Manufacturing Company, Taiwan

IP-P13 Integrated Electronics for an Electromagnetic Energy Harvester in 0.35 μm Standard CMOS Technology:

Arian Rahimi, Middle East Technical University, Turkey

IP-P14 High Vgs MOSFET Characteristics with Thin Gate Oxide for PMIC Application:

Jaehan Cha, Kyungho Lee, Sungoo Kim, Juho Kim, Namkyu Park, Taejong Lee, MagnaChip Semiconductor Ltd., Korea, South

IP-P15 Drift Design Impact on Quasi-Saturation & HCI for Scalable NLD MOS:

Yun Shi^{2}, Natalie Feilchenfeld^{2}, Rick Phelps^{2}, Max Levy^{2}, Martin Knaipp^{1}, Rainer Minixhofer^{1},
^{1}Austriamicrosystems, Austria; ^{2}IBM
Microelectronics, United States

IP-P16 A Versatile 30V Analog CMOS Process in 0.18 μm Technology for Power Management Applications:

Yongkeon Choi, Dongbu HiTek, Korea, South

WBG-P1 Lateral AlGaN/GaN SBDs with Reduced on Resistance:

Woochul Jeon^{2}, Younghwan Park^{2}, Jaehoon Park^{2}, Shinwhan Hwang^{2}, Junghee Lee^{1}, Kiyeol Park^{2}, ^{1}Kyungpook National University, Korea, South; ^{2}Samsung Electro-Mechanics, Korea, South

WBG-P2 3.7 mOhm-cm², 1500 V 4H-SiC DMOSFETs for Advanced High Power, High Frequency Applications:

Lin Cheng, Sarit Dhar, Craig Capell, Anant Agarwal, John Palmour, Cree, Inc., United States

WBG-P3 High Voltage Gan SBD on Si Substrate by Suppressing Metal Spikes:

Min-Woo Ha^{1}, Cheong Hyun Roh^{1}, Hong Goo Choi^{1}, Jun Ho Lee^{1}, Hong Joo Song^{1}, Ogyun Seok^{2}, Cheol-Koo Hahn^{1}, ^{1}Korea Electronics Technology Institute, Korea, South; ^{2}Seoul National University, Korea, South

WBG-P4 Effect of Oxygen Annealing Temperature on AlGaN/GaN HEMTs:

Ogyun Seok, Jiyong Lim, Young-Shil Kim, Min-Koo Han, Seoul National University, Korea, South

WBG-P5 Normally-Off High-Voltage P-Gan Gate Gan HFET with Carbon-Doped Buffer

Oliver Hilt, Frank Brunner, Melanie Ho, Arne Knauer, Eldad Bahat-Treidel, Joachim Wuerfl, Ferdinand-Braun-Institut, Germany

WBG-P6 Second Breakdown in AlGaAs/InGaAs/GaAs HEMT Power Transistors:

Vipindas Pala, Paul Chow, RPI, United States

WBG-P7 A New Vertical Gan SBD Employing in-situ Metallic Gallium Ohmic Contact:

Jiyong Lim, Ogyun Seok, Min-Koo Han, Seoul National University, Korea, South

WBG-P8 High Breakdown Voltage AlGaN/GaN HEMTs by Employing Selective Fluoride Plasma Treatment:

Young Shil Kim, Jiyong Lim, Ogyun Seok, Min Koo Han, Seoul National University, Korea, South

PK-P1 Design and Characterization of a 3D Half-Bridge Semiconductor Power Module in a DFN3x3 Package for DC-DC Buck Converter Application:

Yi Su, Anup Bhalla, Daniel Ng, Fei Wang, Jonathan Xue, Ji Pan, Alpha and Omega Semiconductor INC, United States

PK-P2 Electrical Reliability of Au-In Transient Liquid Phase Bonding for SiC Power Semiconductor Devices:

Brian Grummel^{2}, Habib Mustain^{2}, John Shen^{2}, Allen Hefner^{1}, ^{1}NIST, United States; ^{2}University of Central Florida, United States

PK-P3 Thermal Impedance Spectroscopy of Power Modules During Power Cycling:

Alexander Hensler^{1}, Christian Herold^{1}, Josef Lutz^{1}, Markus Thoben^{2}, ^{1}Chemnitz University of Technology, Germany; ^{2}Infineon Technologies AG, Germany

PK-P4 Application Driven Integrated Design of a Half-Bridge Power Switch:

Adane Solomon, Alberto Castellazzi, University of Nottingham, United Kingdom

PK-P5 Investigations on Wirebond-Less Power Module Structure with High-Density Packaging and High Reliability:

Yoshinari Ikeda^{1}, Masafumi Horio^{1}, Tetsuya Inaba^{2}, Motohito Hori^{2}, Yoshikazu Takahashi^{2}, ^{1}Fuji Electric Holdings Co., Ltd., Japan; ^{2}Fuji Electric Systems Co., Ltd., Japan

7:00-10:00pm Conference Dinner Party

Wednesday May 25, 2011

9:00am-10:15am Session 7
GaN Power Devices

Chairs: **Min-Koo Han**, Seoul National University
Peter Moens, On Semiconductor

9:00am-9:25am
A Novel Normally-Off Gan Power Tunnel Junction FET:

Li Yuan, Hongwei Chen, Qi Zhou, Chunhua Zhou, Kevin J. Chen, Hong Kong University of Science and Technology, Hong Kong

9:25am-9:50am
Gan Based Super HFET Over 700V Using Polarization Super-Junction Concept:

Akira Nakajima^{2}, Yasunobu Sumida^{1}, Mahesh Dhyani^{2}, Hiroji Kawai^{1}, Sankara Narayanan Ekkanath Madathil^{2}, ^{1}POWDEC K.K., Japan; ^{2}University of Sheffield, United Kingdom

9:50am-10:15am
Over 1.7 kV Normally-Off Gan Hybrid MOS-HFETs with a Lower on-Resistance on a Si Substrate:

Nariaki Ikeda, Ryosuke Tamura, Takuya Kokawa, Hiroshi Kambayashi, Yoshihiro Sato, Takehiko Nomura, Sadahiro Kato, Advanced Power Device Research Association, Japan

10:15am-10:40am Break

10:40am-12:20pm Session 8

SiC Power Devices

Chairs: Jose Milan, CNM
David Sheridan, Semisouth Inc.

10:40am-11:05am

**Low on-Resistance 1.2 kV 4H-SiC MOSFETs
Integrated with Current Sensor:**

Akihiko Furukawa, Shinichi Kinouchi, Hiroshi Nakatake,
Yuji Ebiike, Yasuhiro Kagawa, Naruhisa Miura,
Yukiyasu Nakao, Masayuki Imaizumi, Hiroaki Sumitan,
Mitsubishi Electric Corporation, Japan

11:05am-11:30am

**4H-SiC Bipolar Junction Transistors with Record
Current Gains of 257 on (0001) and 335 on (000-1):**

Hiroki Miyake, Tsunenobu Kimoto, Jun Suda, Kyoto
University, Japan

11:30am-11:55am

**5kV Class 4H-SiC Pin Diode with Low Voltage
Overshoot During Forward Recovery for High
Frequency Inverter:**

Shuji Ogata, Yoichi Miyanagi, Koji Nakayama, Atsushi
Tanaka, Katsunori Asano, The Kansai Electric Power
Co., Inc., Japan

11:55am-12:20pm

**A SiC Static Induction Transistor (Sit) Technology for
Pulsed RF Power Amplifiers:**

Francis Chai{1}, Bruce Odekirk{1}, Ed Maxwell{1},
Mar Caballero{2}, Terri Fields-Weisman{1}, Mike
Mallinger{2}, Dumitru Sdrulla{1}, {1}PPG, United
States; {2}RFIS, United States

12:20pm-2:00pm Lunch Break

2:00pm-3:40pm Session 9

High Voltage MOSFETS

Chairs: **Vijay Parthasarathay**, Power Integrations
Deva Pattayanak, Vishay-Siliconix

2:00pm-2:25pm

UltiMOS : a Local Charge Balanced Trench-Based 600V Super-Junction Device:

Peter Moens, Filip Bogman, Hocine Ziad, Herbert Devleeschouwer, Marnix Tack, Gary Loechelt, Gordy Grivna, John Parsey, Peter Zdebel, On Semiconductor, United States

2:25pm-2:50pm

Vertical Charge Balance Effect on 600V Class Trench-Filling Superjunction Power MOSFETS

Tomohiro Tamaki, Yoshito Nakazawa, Hideo Kanai, Yuya Abiko, Yuta Ikegami, Michio Ishikawa, Eiji Wakimoto, Takeshi Yasuda, Satoshi Eguchi, Renesas Electronics Corporation, Japan

2:50pm-3:15pm

Energy Limits for Unclamped Inductive Switching in High-Voltage Planar and Superjunction Power MOSFETS

Jaume Roig, Peter Moens, Jason McDonald, Piet Vanmeerbeek, Filip Bauwens, Marnix Tack, On-Semiconductor, Belgium

2:50pm-3:15pm

Improvement of Switching Trade-Off Characteristics Between Noise and Loss in High Voltage MOSFETS

Wataru Saito, Satoshi Aida, Shigeo Koduki, Masaru Izumisawa, Toshiba Corp., Japan

3:40pm-4:10pm **Break**

4:10pm-5:50pm Session 10

Packaging and Module Technologies

Chairs: **John Shenan**, University of Central Florida
Dieter Silber, University of Bremen

4:10pm-4:35pm

300A, 650V, 70 Um Thin IGBTs with Double-Sided Cooling:

Hsueh-Rong Chang, Jiankang Bu, George Kong, Ricky Labayen, International Rectifier, United States

4:35pm-5:00pm

Skin: Double Side Sintering Technology for New Packages:

Thomas Stockmeier, Peter Beckedahl, Christian Goebel, Thomas Malzer, Semikron Elektronik GmbH & Co. KG, Germany

5:00pm-5:25pm

A Novel Power System in Package with 3D Chip on Chip Interconnections of the Power Transistor and its Gate Driver:

Timothe Simonot, Rouger Nicolas, Crebier Jean-Christophe, Gaude Victor, G2Elab, France

5:25pm-5:50pm

Innovative Heat Removal Structure for Power Devices - the Drift Region Integrated microchannel Cooler

Kremena Vladimirova, Jean-Christophe Crebier, Yvan Avenas, Christian Schaeffer, G2Elab, France

Thursday May 26, 2011

8:30am-10:10am Session 11
Device and Process Reliability

Chairs: Il_Yong Park, Dongbu
Ronghua Zhu, Maxim

8:30am-8:55am
Interface Charge Trapping and Hot Carrier Injection
in High Voltage SOI SJ LDMOSFET:
Marina Antoniou^{1}, Florin Udrea^{1}, Elizabeth Kho
Ching Tee^{2}, Yang Hao^{2}, Kee Yaw Kia^{2}, Steven
Pilkington^{2}, Deb Kumar Pal^{2}, Alexander
Hoelke^{2},^{1}University of Cambridge, United
Kingdom; ^{2}XFAB Sarawak Sdn. Bhd, Malaysia

8:55am-9:20am
Reliability and Performance Optimization of 42V N-
Channel MOS Drift Transistor in Advanced BCD
Technology:
Antonio Molfese, Giansalvo Pizzo, Paolo Gattari, Giulio
Marchesi, Giuseppe Croce, STMicroelectronics, Italy

9:20am-9:45am
Practical Approaches to Improve Thermal SOA for
Smart Power IC:
Tetsuya Nitta^{1}, Akira Omichi^{1}, Keiichi Furuya^{2},
Shinichiro Yanagi^{1}, Yasuki Yoshihisa^{1}, Takashi
Kuroi^{1}, Kenichi Hatasako^{1}, Shigeto
Maegawa^{1},^{1}Renesas Electronics Corp., Japan;
^{2}Renesas Semiconductor Engineering Corp., Japan

9:45am-10:10am
Rob van Dalen^{1}, Siddhartha Dhar^{2}, Anco
Heringa^{2}, Maarten Swanenberg^{1}, Arnold van der
Wal^{1}, Priscilla Boos^{1}, Valerie Braspenning-
Girault^{1},^{1}NXP, Netherlands; ^{2}NXP Research,
Belgium

10:10am-10:30am Break
10:40am-12:20pm Session 12

Smart Power Circuits

Chairs: **Sujit Banerjee**, Power Integrations
Wai Tung Ng, University of Toronto

10:40am-11:05am

A Novel Silicon-Embedded Coreless Transformer (Sect) for Isolated DC-DC Converter Application:

Rongxiang Wu^{2}, Johnny K.O. Sin^{2}, S.Y. Ron Hui^{{1}, {1}} City University of Hong Kong, Hong Kong; ^{2} Hong Kong University of Science and Technology, Hong Kong

11:05am-11:30am

Integrated Low Power and High Bandwidth Optical Isolation for Power MOSFETs:

Nicolas Rouger, Jean-Christophe Crébier, Olivier Lesaint, Grenoble Electrical Engineering Lab / CNRS, France

11:30am-11:55am

Design and Characterization of an Integrated Coreless Transformer Onto a CMOS Gate Driver for Gate Signal Insulation Purposes:

Timothe Simonot^{1}, Jean-Daniel Arnould^{2}, Nicolas Rouger^{1}, Jean-Christophe Crebier^{{1}, {1}} G2Elab, France; ^{2} IMEP-LAHC, France

11:55am-12:20pm

Reduction of Conducted Electromagnetic Interference in SMPS Using Programmable Gate Driving Strength:

Andrew Shorten^{2}, Armin Akhavan Fomani^{2}, Wai Tung Ng^{2}, Haruhiko Nishio^{1}, Yoshikazu Takahashi^{{1}, {1}} Fuji Electric Systems Co. Ltd., Japan; ^{2} University of Toronto, Canada

12:20pm-2:00pm

Lunch Break

2:00pm-3:40pm Session 13

Low Voltage Power Devices

Chairs: **Jan Sonsky**, NXP
Andy Strachan, National Semiconductor

2:00pm-2:25pm

Self Heating Analysis of Power MOSFET Module During Burn-in Test:

Evgueniy Stefanov^{2}, Rene Escoffier^{1}, Gael
Blondel^{3}, Blaise Rouleau^{3}, ^{1}CEA-LETI, France;
^{2}FREESCALE Semiconductor, France; ^{3}VALEO
VES, France

2:25pm-2:50pm

Design of an 80V-Class High-Side Compatible Double Resurf JI L-IGBT

Hiroki Fujii, Shinichi Komatsu, Masaharu Sato,
Toshihiko Ichikawa, Renesas Electronics Corporation,
Japan

2:50pm-3:15pm

150V, 100mOhm, SOI Power LDMOS with High Avalanche Current Capability for MHz Frequency Power Switching Applications

Patrick Shea, John Shen, University of Central Florida,
United States

3:15pm-3:40pm

P-Type Isolated GGNMOS with Deep Current Path for ESD Protection

Jae-Hyun Yoo, Jongmin Kim, Joonghyeok Byeon,
Youngsang Son, Jaeyoung Park, Won-Young Jung,
Dongbu Hitek, Korea, South

3:40pm-4:00pm Closing Remarks and Awards